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Characterisation of DST Delay Trigger Units

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ABSTRACT

This paper reports on tests conducted to validate the accuracy of Defence Science and Technology Group, Maritime Division's Delay Trigger Units (DTUs). The DTUs are designed to generate voltage signals to activate (trigger) external devices, such as firing units, high speed video, and data acquisition equipment in a predetermined and precise time sequence to permit the capture of data from transient events. To ensure the validity of the data obtained, the accuracy of the DTUs was evaluated against design specifications. The tests show that the DTUs met the specified requirements for the delay and rise times of the trigger signals from both the transistor to transistor logic (TTL) output signal and the 100 volt capacitor discharge output signal.

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Characterisation of DST Delay Trigger Units

Executive Summary

This paper reports on tests conducted to validate the accuracy of Defence Science and Technology Group's Maritime Division Delay Trigger Units (DTUs) against specified design requirements. The DTUs are required to generate voltage signals to activate (trigger) acquisition and imaging systems in a predetermined and accurate time sequence before initiating an event, such as an explosive charge detonation. An accurate time sequence ensures that valid data is captured and subsequent data analysis allows the determination of a time zero datum and hence the arrival times of a shock response at the specific point of interest within or around a structure or in the free field.

The evaluation of the DTU against the design specifications has shown that the DTUs met the design requirements. This includes conforming to the operational requirements in terms of the delay and rise times of the trigger signals for the transistor to transistor logic (TTL) output signals, and for 100 volt capacitor discharge output signals.

The DTUs will be used in experiments to capture data associated with assessing the response of structures, equipment and human systems to dynamic loading conditions to support the Australian Defence Force (ADF).

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1. Introduction

Delay Trigger Units (DTU) are designed to generate voltage signals at accurate pre-set time intervals to enable high speed data acquisition devices to be activated (triggered) in a predetermined and precise time sequence. They are used in conjunction with various data and image recording systems to measure and record parameters associated with the detonation of explosives (both in air and underwater) as well as the response of structures to these loads.

It is imperative when capturing high speed transient data associated with explosive events, that the recording devices are triggered at precise, predetermined time intervals before the event to ensure capture of the relevant data. The subsequent analysis also requires an accurate time zero datum to measure the arrival times of a shock wave at the specific point of interest within a structure or in the free field.

The DTU manual [1] documents the specification requirements, set by Maritime Division (MD) and Weapons & Combat Systems Division (WCSD), for the system. The specification limits were chosen to ensure accurate blast data and arrival times. As some of the data recording systems have sampling rates in the order of five million samples per second, it was desirable that the overall accuracy of the DTU is greater than one sample period, i.e. less than 200 ns. As the total error is the sum of the components, tight tolerances were specified for each variable i.e. rise times and time between the immediate and delay outputs.

MD and WCSD contracted Scientific and Engineering Services (SES) at Edinburgh, South Australia, to manufacture a number of DTUs to support field and laboratory experiments. The SES design incorporated modifications and improvements to a previously designed DTU used by MD. MD took delivery of three units labelled 8, 9 and 10; all three units were evaluated to ensure they met the design specifications and user requirements.

1.1 Delay Trigger Unit

The DTU documentation [1] provides details of the various controls, signal interfaces, operational instructions and system specifications including the accuracy requirements of the actual delay times and the requisite rise times. The time delay between the immediate and delay output signals can be programmed to produce trigger signals (output voltages) which have precise delay times ranging from 0 to 99 seconds in increments of 1μs. The DTU can then be armed by pushing the two arm buttons in unison. After a few seconds the green Light Emitting Diode (LED) on the arm buttons will illuminate followed shortly (approximately 1 – 2 seconds) by the two red LED's above the CAP (100 volt Capacitor exponential discharge voltage) output terminals to indicate the capacitors are charged to the required voltage and are ready for activation. Figure 1 shows the DTU tested. An illustration of the front panel is shown in Figure 2. The DTU can be activated (triggered) manually, using the "trigger" button or by an external signal via any one of the three input terminals labelled as RELAY (short circuit), CAP (100 volt) capacitor discharge pulse) and

TTL (transistor to transistor logic, 5 volts). These are highlighted in the blue area of Figure 2.

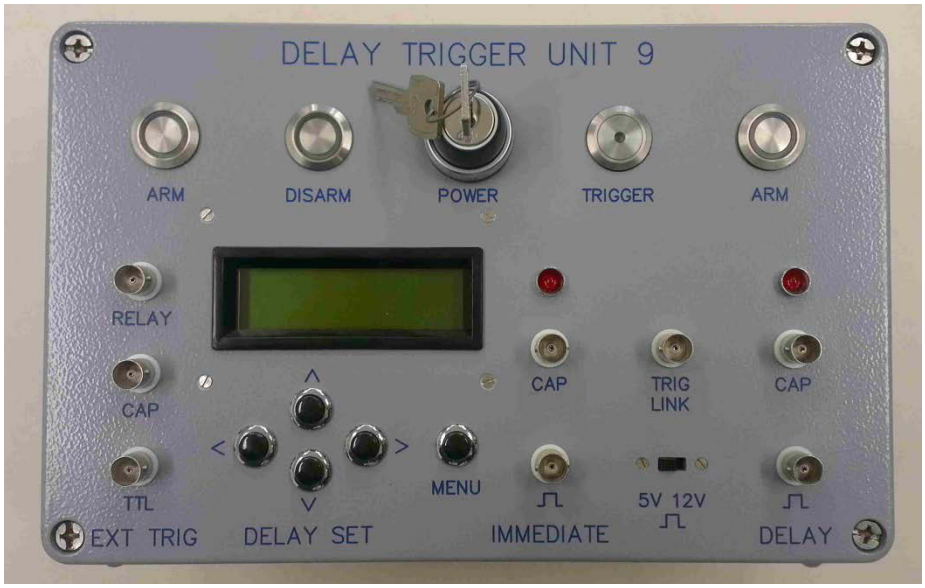

Figure 1: Delay Trigger Unit

When triggered, the DTU produces four voltage outputs. Two are positive TTL square waveforms from each of the immediate and delay TTL terminals 2 and 4 respectively. The other two are exponential waveforms from each of the immediate and delay CAP terminals 1 and 3 respectively.

The immediate CAP and TTL and the delay CAP and TTL terminals are highlighted in the green and orange areas respectively, Figure 2, and are labelled terminals 1 to 4.

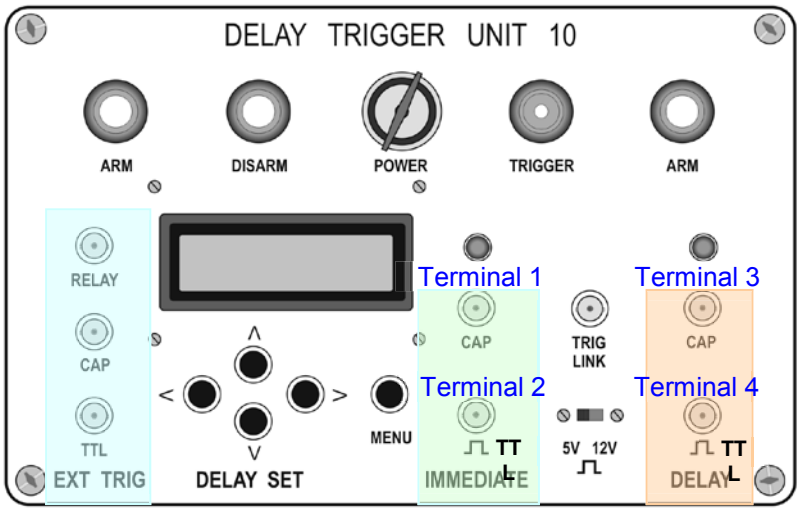

Figure 2: Schematic of the Delay Trigger Unit Front Panel

2. Aim

The objective of these tests was to characterise the performance of each of the three DTUs in order to ensure they met the design specifications and user requirements.

The specific aims were to:

1. Determine the accuracy of the output delay pulses relative to the pre-set delay time for the immediate and delay TTL voltage outputs (terminals 2 and 4 respectively) and the immediate and delay CAP voltage outputs (terminals 1 and 3 respectively)
2. Determine the accuracy of the timing synchronisation between the immediate CAP and TTL output voltage pulses (terminals 1 and 2 respectively) and, the delay CAP and TTL outputs voltage pulses (terminals 3 and 4 respectively)
3. Determine the average rise time of the voltage pulses for both TTL and CAP outputs.

3. Methodology and Results

Two digital measuring devices were used to evaluate the DTUs. A Tektronix Mixed Signal Oscilloscope (MSO), Model MSO4034 (Figure 3) and a Keysight Universal Frequency counter (UFC) Model 53220A (Figure 4).

3.1 Tektronix Mixed Signal Oscilloscope (MSO) - Model MSO4034

The MSO specifications include; 350 MHz Bandwidth, 4 Analog + 16 Digital channels 2.5 GS/s Sample rate, Mixed Signal Oscilloscope.

The MSO allows signals from transient events to be captured and signal parameters to be measured. Signals are represented in a two-dimensional form allowing the amplitude of the signal to be read on the "Y" axis and the duration of the event on the "X" axis. The MSO can show the shape and distortion of the signal, the relative timings of the acquired signals and rise times.

The MSO was configured to capture both the DTU Immediate output pulses (terminals 1 and 2) and the Delay output pulses (terminals 3 and 4).

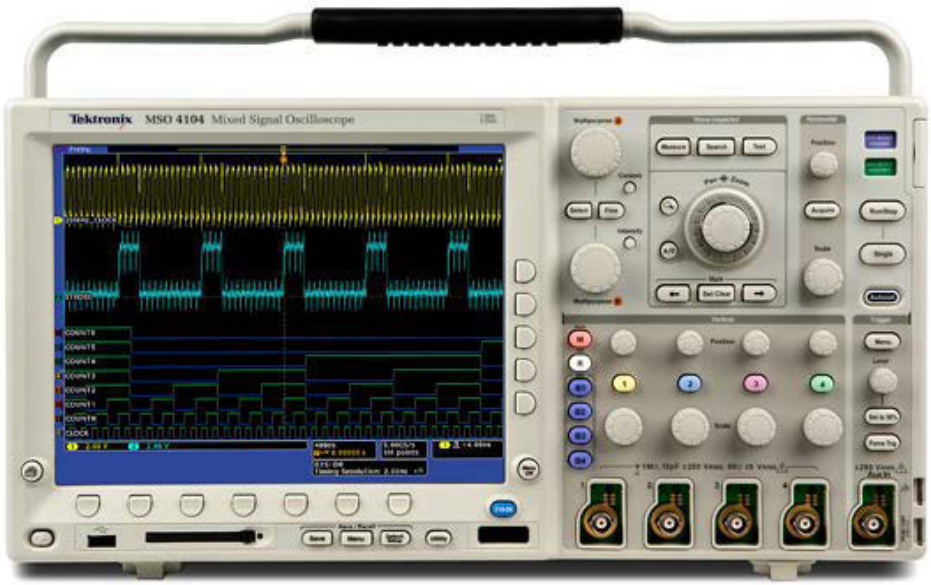

Figure 3: Tektronix MSO 4034 Digital Storage Oscilloscope

The MSO was configured to conduct automated measurements which removes the user error element and allows repeatability so that multiple measurements can be conducted quickly and accurately.

The following "Auto" functions were used:

1. Rising edge to Rising edge function to measure the synchronisation delay between both the immediate voltage output pulses (terminals 1 and 2) as well as the delayed voltage output pulses (terminals 3 and 4).
2. The rise time function to measure the time for each voltage input pulse from low to high signal level.

The MSO was not suitable to evaluate the pre-set time delays using the auto function due to its decreasing accuracy as the pre-set delay times are increased. The Keysight Universal Frequency counter was selected to make these measurements more accurately.

3.2 Keysight Universal Frequency Counter (UFC) – Model 53220A

The 53220A 350 MHz universal frequency counter/timer is a two-channel frequency counter. The UFC measures frequency and time intervals, has a 12 digits/second resolution and 100 ps time interval resolution. The UFC was configured to make time interval measurements between the DTU Immediate and Delayed outputs.

Figure 4: Keysight 53220A Universal Frequency counter (UFC)

3.3 Pre-set delay time accuracy

The Universal Frequency Counter (UFC) was used to evaluate the accuracy of the pre-set time delay outputs. Nine delay times ranging from 0 seconds to 10 seconds were evaluated for each of the DTUs. Ten measurements were recorded for each of the pre-set delay times with the TTL output (terminals 2 and 4) connected to the UFC and again with the CAP output (terminals 1 and 3) connected. The immediate CAP and delay CAP outputs were connected using a 10X voltage attenuator and setting the voltage full range to 500 V. The immediate TTL and delay TTL outputs were connected to the UFC and setting the voltage full range to 50 V.

The delay time error is the difference between the pre-set delay time and actual measured delay time. A negative difference is when the measured time is less than the pre-set time delay. A positive difference is when the measured time is greater than the pre-set delay time. The complete list of Pre-set delay time measurements is included in Appendix A. Table 1 lists the average delay time errors for each DTU.

Table 1: Time difference between the pre-set delay time and the measured times

Pre-set delay time average error between Immediate and Delay outputs (TTL Terminals 2 & 4, CAP Terminals 1 & 3)							
	DTU 8		DTU 9		DTU 10		
Delay Time	TTL	CAP	TTL	CAP	TTL	CAP	Expected Error ± (ns)
	Average Delay Error (ns)						
0 µs	5	5	0	0	-5	5	20
1 µs	24	26	20	21	16	25	40
10 µs	79	79	75	76	70	79	100
100 µs	25	24	19	20	15	24	100
1 ms	359	743	678	807	666	870	100
10 ms	262	677	592	781	707	548	100
100 ms	475	780	796	766	145	467	1 µ
1 s	78	–236	634	–1089	–6202	–3387	1 µ
10 s	16 950	13 260	3615	5807	–16 282	–18 342	1 µ

3.4 Output pulse synchronisation

The DTU provides two types of output signals commensurate with the triggering requirements of the systems being used. One type is the TTL that delivers a 5 volt square wave signal used to trigger various acquisition and imaging systems. The other type is based on a capacitor discharge circuit and delivers a 100 V dc positive signal with an exponential decay. This is usually used to trigger firing units that initiate explosives or flash lighting arrays for imaging systems. An illustration of the two trigger signals is shown in Figure 5.

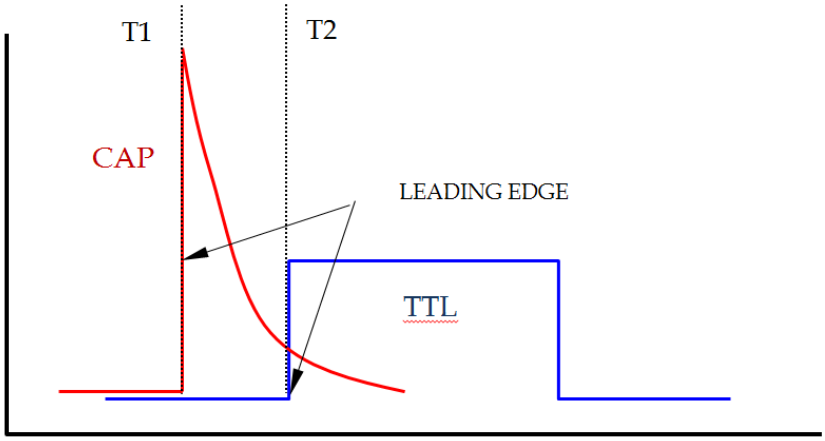

Figure 5: TTL waveform (blue) and CAP waveform (red) (Not to scale)

If no pre-set delay time is required, i.e. the simultaneous initiation of an explosive event and activation of an acquisition system, the immediate TTL and CAP output signal leading edges should coincide. Likewise the delay TTL and CAP output signal leading edges should also coincide. The extent to which the leading edges coincide needs to be quantified to ensure that valid data is captured.

The method used to quantify the data was to measure the difference in time (T1 and T2) of the leading edge of the two signals. Once the signals were captured, the time between the leading edges was measured by the Auto function of the MSO. To attain quantitative data 10 tests were conducted of each measurement for all units.

The TTL and CAP outputs were connected to the MSO set at a sampling rate of 2.5 Giga-samples/sec, being the maximum resolution to accurately measure any difference between the times (T1 and T2) of the leading edges of the signals and hence determine any error. To capture and display the four DTU outputs together, the DTU pre-set delay was set to 10 µs.

Table 2 lists the average time difference in nanoseconds (ns) between the Immediate CAP and TTL signal leading edges and the average time difference between the Delayed CAP and TTL signal leading edges. A negative difference indicates the TTL signal leading edge occurring before the CAP signal leading edge. A positive difference indicates the CAP signal leading edge occurring before the TTL signal leading edge. The complete list of synchronisation measurements is located in Appendix B and a sample of the captured signals is shown in Figure 6.

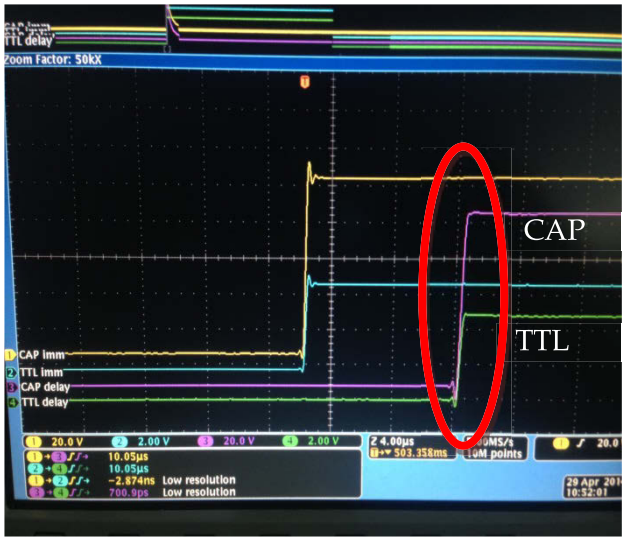

Figure 6: MSO capture of Immediate CAP and TTL outputs and Delay CAP and TTL outputs (circled)

Table 2: Summary of synchronisation time errors measured between CAP and TTL outputs

Synchronisation error between CAP and TTL outputs							
	DTU 8		DTU 9		DTU 10		
Delay Time	Immediate	Delay	Immediate	Delay	Immediate	Delay	Specification Limit (ns)
	Average Sync Error (ns)						
0 µs	3	6	7	7	8	3	10
1 µs	2	6	5	7	7	2	
10 µs	2	6	5	7	7	2	
100 µs	2	6	6	7	7	2	
1 ms	3	4	5	6	7	1	
10 ms	2	6	4	7	6	1	
100 ms	2	7	5	6	7	1	
1 s	–7	–7	0	–7	–3	1	

3.5 Waveform Rise Time Measurements

The rise time of a signal is an important consideration to ensure that valid data is obtained, particularly when measuring fast transient events associated with air and underwater blast.

In electronics when describing voltage amplitude, rise time (T1-T2 or T3-T4), refers to the time required for a voltage signal to change from a specified low value to a specified high value, see Figure 7. Typically these values are 10% and 90% of the height of the signal respectively. In this report the rise time was calculated from the time measured at 0% (0 V baseline) to the time measured at 100% of the height of the signal.

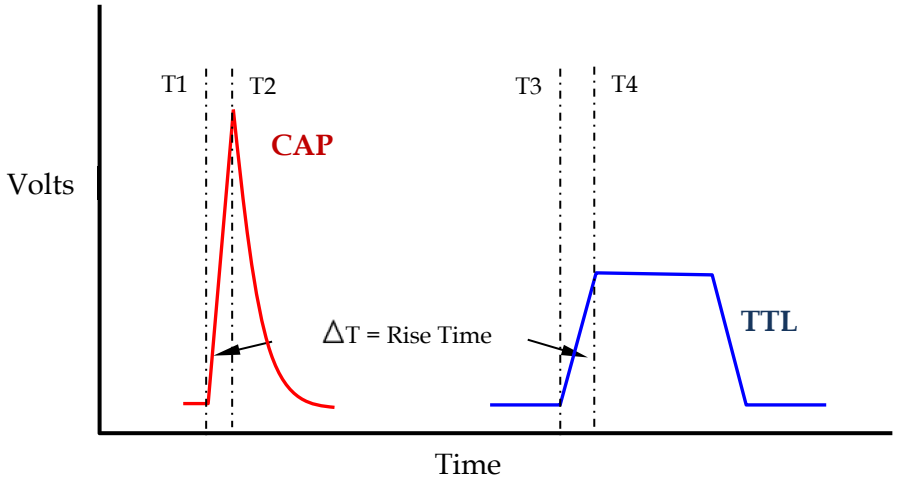

Figure 7: Illustration of a Rise time for a CAP output and a TTL output signal

The equipment requiring activation could be triggered from any part of the leading edge between (0% and 100%) of the trigger signal. Thus to reduce the potential error in the triggering of different equipment, the time difference between the lower and upper values should be as small as possible. As the delta between the two measurements decreases so does the potential error and this is particularly important when recording data for fast transient events.

A large time difference between the lower and upper values of a particular trigger signal would also adversely affect the difference, hence error, between the pre-set delay time and the delivered delay time.

To confirm that the rise time is independent of the pre-set delay time on the DTU, a number of nominal pre-set times, up to 1ms were evaluated. Pre-set delay times greater than 1 ms were not evaluated as a lower DSO sample rate would be required to capture both immediate and delay outputs on the same screen. The resulting resolution would be too low to accurately measure any time differences.

Tables 3 and 4 list the average measured rise times in nanoseconds (ns) for the CAP and TTL output signals. The rise time value is the difference between T1 to T2 for the CAP outputs and between T3 to T4 for the TTL output. The complete list of rise time measurements is included in Appendix C.

Table 3: Summary of CAP output rise-times for each DTU

	Immediate	Delay	Immediate	Delay	Immediate	Delay	
	16	19	16	20	16	19	
	17	19	15	20	16	20	
	17	19	16	20	16	20	50
	16	19	16	20	16	20	
	17	19	16	20	16	20	

Table 4: Summary of TTL output rise-times for each DTU

TTL Output Rise time measurements (Terminals 2 & 4)							
	DTU 8		DTU 9		DTU 10		
Delay Time	Immediate	Delay	Immediate	Delay	Immediate	Delay	Specification Limit (ns)
	Rise time average (ns)						
0 µs	14	16	13	16	15	16	
1 µs	14	17	14	18	14	17	
10 µs	13	17	14	19	14	17	20
100 µs	14	17	14	19	15	17	
1 ms	13	17	14	19	15	17	

4. Discussion and Conclusion

The Delay Trigger Unit design specification tolerance limits [1] were stipulated to ensure that the cumulative maximum timing errors of the DTUs were less than 200 ns (less than 1 sample period) when the acquisition system is sampling at 5 million samples/s. This is the maximum sample rate of some of the acquisition systems used at DST (Melbourne) to measure blast parameters.

The accuracy of the DTU pre-set delay time measured between the immediate and delay TTL and CAP output signals was found to meet the specified tolerance limit [1] for pre-set delays from 0 μs to 100 μs, see Table 1. Compliance with the specified tolerances for longer pre-set times, 1 ms to 10 s, was not met. This is due to the accumulation of errors within the DTU frequency clock counter and crystal circuitry. This error, considered normal, increases as the delay period increases. However this is of an acceptable level being less than 0.1% error of the pre-set delay times.

The specified tolerance limit for the zero delay times of the CAP and TTL output signals was met for each DTU. All measured timing errors were less than the specified limit [1] of 20 ns, Table 1 and Appendix A.

The specified tolerance limit for the synchronisation between the TTL and CAP output signals (Immediate and Delay) was met for each DTU. The immediate and delay output signals measured less than the specified limit [1] of 10 ns, Table 2 and Appendix B.

The specified rise time limits for CAP output signals were met for each DTU. The signals delivered by the immediate and delay CAP output measured less than the specified design tolerance limits [1] of 50 ns, Table 3 and Appendix C.

The specified rise time limits for TTL output signals were met for each DTU. The signals delivered by the immediate and delay TTL output measured less than the specified design tolerance limits [1] of 20 ns, Table 4 and Appendix C.

The evaluation of the DTU characteristics and performance has shown that the delay trigger units provide the requisite accuracy in terms of the delay times and the rise time of the signals required to trigger acquisition systems that can record up to 5 million samples a second. It is concluded that the accuracy of the DTUs is within requirements for recording transient events.

References

1. Operation and Technical Manual “Delay Trigger Unit” SES DSTO P498, V1.1 Dated 29 June 2009.
2. User Manual, Tektronix MSO 4034 Mixed Signal Oscilloscope.
3. User Manual, Keysight Universal Frequency Counter – Model 53220A.

Appendix: A

The tables below list the Delay time errors in nanoseconds (ns) for each DTU. The Delay time error is the difference between the pre-set delay time and actual measured delay time.

A.1 DTU 8 Pre-set delay time errors

Pre-set delay time errors measured from the TTL outputs (Terminals 2 & 4)											
DTU 8											
Delay Time	Delay time error (ns)										Average Timing Error (ns)
	1	2	3	4	5	6	7	8	9	10	
0 µs	6	5	6	6	3	4	3	4	6	4	5
1 µs	26	22	25	24	25	24	22	25	25	25	24
10 µs	79	79	80	79	78	79	78	81	79	80	79
100 µs	25	24	25	25	26	24	26	25	24	24	25
1 ms	232	870	231	230	232	229	233	871	230	233	359
10 ms	101	101	101	101	743	101	103	104	743	424	262
100 ms	217	858	859	219	221	218	220	219	860	859	475
1 s	–212	435	–199	–187	–176	–165	470	–153	479	484	78
10 s	16 397	16 772	16 158	17 120	17 278	16 839	16 853	17 007	17 829	17 245	16 950

Pre-set delay time errors measured from the CAP outputs (Terminals 1 & 3)											
DTU 8											
Delay Time	Delay time error (ns)										Average Timing Error (ns)
	1	2	3	4	5	6	7	8	9	10	
0 µs	7	5	4	6	3	5	4	4	6	5	5
1 µs	25	25	26	25	25	26	25	26	26	27	26
10 µs	78	79	80	79	79	79	79	78	79	79	79
100 µs	24	23	25	24	24	24	23	23	24	24	24
1 ms	232	871	870	871	871	870	869	231	870	870	743
10 ms	100	741	741	739	740	742	742	741	741	741	677
100 ms	201	845	847	844	842	846	847	843	842	844	780
1 s	–366	–361	–352	270	278	–372	–370	–360	–358	–368	–236
10 s	13 973	13 392	14 083	12 572	12 542	12 444	13 519	12 867	13 613	13 594	13 260

A.2 DTU 9 Pre-set delay time errors

Pre-set delay time errors measured from the TTL outputs (Terminals 2 & 4)											
DTU 9											
Delay Time	Delay time error (ns)										Average Timing Error (ns)
	1	2	3	4	5	6	7	8	9	10	
0 µs	–1	–2	0	–1	1	1	1	–1	0	0	0
1 µs	21	19	19	19	20	21	18	19	19	20	20
10 µs	75	75	76	75	75	73	74	73	76	76	75
100 µs	21	18	19	19	20	19	19	20	19	18	19
1 ms	869	870	232	871	869	869	230	230	872	868	678
10 ms	783	781	785	785	146	784	783	783	143	145	592
100 ms	289	1065	1065	1063	1065	425	426	427	1066	1067	796
1 s	744	750	755	760	762	123	765	772	134	778	634
10 s	1726	2349	2651	2956	3303	3638	3995	5084	5400	5051	3615

Pre-set delay time errors measured from the CAP outputs (Terminals 1 & 3)											
DTU 9											
Delay Time	Delay time error (ns)										Average Timing Error (ns)
	1	2	3	4	5	6	7	8	9	10	
0 µs	–1	–1	1	0	0	1	1	0	0	2	0
1 µs	20	22	21	22	20	21	21	21	22	21	21
10 µs	78	76	76	76	75	77	74	73	75	75	76
100 µs	20	21	21	21	19	21	20	20	21	20	20
1 ms	232	871	872	871	871	870	872	869	870	868	807
10 ms	780	780	780	781	780	781	780	782	780	782	781
100 ms	889	871	892	893	894	256	899	259	901	904	766
1 s	–886	–849	–825	–804	–1423	–756	–1375	–1351	–1324	–1300	–1089
10 s	4024	5153	4726	5568	4384	5583	5112	7352	7998	8173	5807

A.3 DTU 10 Pre-set delay time errors

Pre-set delay time errors measured from the CAP outputs (Terminals 2 & 4)											
DTU 10											
Delay Time	Delay time error (ns)										Average Timing Error (ns)
	1	2	3	4	5	6	7	8	9	10	
0 µs	–3	–5	–4	–6	–4	–6	–5	–5	–6	–4	–5
1 µs	17	15	16	16	14	15	17	17	16	14	16
10 µs	71	71	70	70	71	71	71	68	69	70	70
100 µs	16	15	16	14	14	15	14	14	12	15	15
1 ms	860	218	855	215	858	857	857	860	857	219	666
10 ms	719	718	721	693	695	695	696	697	698	741	707
100 ms	–124	–123	523	526	528	–111	–107	534	–103	–98	145
1 s	–6962	–6759	–6086	–6057	–6033	–6004	–5962	–5908	–6518	–5728	–6202
10 s	–15 763	–16 431	–15 466	–15 208	–17 453	–17 216	–16 484	–16 314	–16 064	–16 421	–16 282

Pre-set delay time errors measured from the CAP outputs (Terminals 1 & 3)											
DTU 10											
Delay Time	Delay time error (ns)										Average Timing Error (ns)
	1	2	3	4	5	6	7	8	9	10	
0 µs	3	5	5	4	5	5	5	5	4	5	5
1 µs	26	25	26	24	25	25	24	25	24	26	25
10 µs	79	80	80	79	80	78	79	79	78	80	79
100 µs	24	23	27	24	25	24	20	25	23	24	24
1 ms	869	871	871	871	870	870	869	869	871	870	870
10 ms	738	739	741	738	100	742	741	740	100	103	548
100 ms	652	15	657	17	19	659	659	662	660	665	467
1 s	–3773	–3738	–3737	–3089	–3705	–3061	–3051	–3033	–3668	–3012	–3387
10 s	–20 784	–19 907	–18 964	–18 567	–18 340	–17 411	–17 832	–17 599	–16 800	–17 218	–18 342

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Appendix: B

The tables below list the measured time differences in nanoseconds (ns) between the Immediate and Delayed CAP and TTL signal leading edges. A negative difference indicates the TTL signal leading edge occurring before the CAP signal leading edge. A positive difference indicates the CAP signal leading edge occurring before the TTL signal leading edge.

B.1 DTU 8 Synchronisation time errors

Synchronisation error between Immediate CAP and TTL outputs (Terminals 1 & 2)											
DTU 8											
Delay Time	Measured time (ns)										Average Sync Error (ns)
	1	2	3	4	5	6	7	8	9	10	
0 µs	2	3	4	2	4	2	3	2	3	3	3
1 µs	4	2	2	2	2	2	2	1	2	2	2
10 µs	1	1	2	2	3	1	1	0	4	3	2
100 µs	2	2	1	3	2	1	2	2	2	4	2
1 ms	2	4	4	3	2	3	2	2	3	4	3
10 ms	2	2	3	–1	–1	3	2	2	2	3	2
100 ms	0	0	–4	18	1	1	–4	–2	17	–3	2
1 s	–8	–7	–4	–5	–4	–6	–4	–18	–6	–6	–7

Synchronisation error between Delay CAP and TTL outputs (Terminals 3 & 5)											
DTU 8											
Delay Time	Measured time (ns)										Average Sync Error (ns)
	1	2	3	4	5	6	7	8	9	10	
0 µs	4	5	5	6	6	6	6	6	6	7	6
1 µs	6	5	8	4	7	6	7	6	8	8	6
10 µs	5	6	4	4	6	7	6	7	7	4	6
100 µs	7	5	6	6	6	6	7	6	7	8	6
1 ms	0	1	5	4	6	5	5	6	7	6	4
10 ms	5	7	5	6	7	6	6	6	4	6	6
100 ms	9	4	6	7	5	5	9	10	6	7	7
1 s	–6	–5	–6	–7	–15	–20	–2	–5	–5	3	–7

B.2 DTU 9 Synchronisation time errors

Synchronisation error between Immediate CAP and TTL outputs (Terminals 1 & 2)											
DTU 9											
Delay Time	Measured time (ns)										Average Sync Error (ns)
	1	2	3	4	5	6	7	8	9	10	
0 µs	8	8	8	7	7	7	6	7	7	6	7
1 µs	6	5	7	6	5	6	5	5	4	5	5
10 µs	5	5	4	5	5	7	6	5	6	4	5
100 µs	6	5	5	6	5	4	7	6	5	7	6
1 ms	5	5	5	5	6	6	5	6	5	6	5
10 ms	4	2	4	4	5	3	5	6	5	5	4
100 ms	3	8	11	10	3	1	5	1	5	–2	5
1 s	1	–1	2	–2	4	–1	0	2	–1	0	0

Synchronisation error between Delay CAP and TTL outputs (Terminals 3 & 5)											
DTU 9											
Delay Time	Measured time (ns)										Average Sync Error (ns)
	1	2	3	4	5	6	7	8	9	10	
0 µs	9	6	7	7	8	9	7	9	7	7	7
1 µs	7	9	8	8	8	8	8	7	7	6	7
10 µs	6	5	8	6	8	8	7	8	8	8	7
100 µs	8	7	9	6	4	8	7	6	7	6	7
1 ms	5	7	7	7	7	8	5	6	6	6	6
10 ms	8	10	6	8	5	7	5	7	8	7	7
100 ms	4	11	9	7	10	3	7	3	2	5	6
1 s	–2	4	–10	–2	–4	–6	–14	–2	–16	–13	–7

B.3 DTU 10 Synchronisation time errors

Synchronisation error between Immediate CAP and TTL outputs (Terminals 1 & 2)											
DTU 10											
Delay Time	Measured time (ns)										Average Sync Error (ns)
	1	2	3	4	5	6	7	8	9	10	
0 µs	9	9	7	7	9	8	7	8	7	8	8
1 µs	8	7	6	7	6	6	8	5	7	8	7
10 µs	8	6	7	7	7	8	7	7	7	7	7
100 µs	9	5	7	8	6	6	7	7	5	8	7
1 ms	8	6	9	6	8	7	8	9	7	8	7
10 ms	7	5	5	8	6	6	7	7	7	4	6
100 ms	7	–11	13	11	13	13	9	4	4	9	7
1 s	6	–3	–11	5	–5	–5	–6	–6	–5	–5	–3

Synchronisation error between Delay CAP and TTL outputs (Terminals 3 & 5)											
DTU 10											
Delay Time	Measured time (ns)										Average Sync Error (ns)
	1	2	3	4	5	6	7	8	9	10	
0 µs	3	2	2	3	4	4	4	3	2	4	3
1 µs	1	2	5	3	1	2	2	2	0	2	2
10 µs	1	2	2	1	1	1	2	2	3	1	2
100 µs	3	2	0	1	2	2	3	1	2	2	2
1 ms	4	2	2	0	0	0	2	1	1	2	1
10 ms	0	2	3	1	1	2	2	2	0	2	1
100 ms	0	1	1	1	1	0	1	3	2	2	1
1 s	12	18	8	3	–6	4	–4	–3	–20	0	1

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Appendix: C

The tables below list the measured rise times in nanoseconds (ns) of the leading edge of the CAP and TTL output signals.

C.1 DTU 8 Output Voltage Rise–times

Rise Time from the immediate CAP output (Terminal 1)											
DTU 8											
Delay Time	Measured rise time (ns)										Average Rise Time (ns)
	1	2	3	4	5	6	7	8	9	10	
0 µs	16	16	16	17	16	16	16	16	16	17	16
1 µs	16	17	17	16	17	17	17	17	17	16	17
10 µs	17	16	17	16	17	16	18	17	17	17	17
100 µs	17	16	17	16	17	16	17	17	17	17	16
1 ms	17	17	17	17	16	17	17	17	17	17	17
Rise Time from the immediate TTL output (Terminal 2)											
DTU 8											
Delay Time	Measured rise time (ns)										Average Rise Time (ns)
	1	2	3	4	5	6	7	8	9	10	
0 µs	16	16	16	17	16	16	16	16	16	17	16
1 µs	16	17	17	16	17	17	17	17	17	16	17
10 µs	17	16	17	16	17	16	18	17	17	17	17
100 µs	17	16	17	16	17	16	17	17	17	17	16
1 ms	17	17	17	17	16	17	17	17	17	17	17
Rise Time from the delay CAP output (Terminal 3)											
DTU 8											
Delay Time	Measured rise time (ns)										Average Rise Time (ns)
	1	2	3	4	5	6	7	8	9	10	
0 µs	16	16	16	17	16	16	16	16	16	17	16
1 µs	16	17	17	16	17	17	17	17	17	16	17
10 µs	17	16	17	16	17	16	18	17	17	17	17
100 µs	17	16	17	16	17	16	17	17	17	17	16
1 ms	17	17	17	17	16	17	17	17	17	17	17
Rise Time from the delay TTL output (Terminal 4)											
DTU 8											
Delay Time	Measured rise time (ns)										Average Rise Time (ns)
	1	2	3	4	5	6	7	8	9	10	
0 µs	16	16	16	17	16	16	16	16	16	17	16
1 µs	16	17	17	16	17	17	17	17	17	16	17
10 µs	17	16	17	16	17	16	18	17	17	17	17
100 µs	17	16	17	16	17	16	17	17	17	17	16
1 ms	17	17	17	17	16	17	17	17	17	17	17

C.2 DTU 9 Output Voltage Rise–times

Rise Time from the immediate CAP output (Terminal 1)											
DTU 9											
Delay Time	Measured rise time (ns)										Average Rise Time (ns)
	1	2	3	4	5	6	7	8	9	10	
0 µs	16	15	15	15	16	16	15	16	16	15	16
1 µs	16	16	16	15	6	15	16	16	16	15	15
10 µs	15	16	16	16	16	15	15	16	16	15	16
100 µs	15	15	16	16	15	16	16	16	16	15	16
1 ms	16	16	16	16	16	16	16	16	16	16	16
Rise Time from the immediate TTL output (Terminal 2)											
DTU 9											
Delay Time	Measured rise time (ns)										Average Rise Time (ns)
	1	2	3	4	5	6	7	8	9	10	
0 µs	13	13	13	13	13	13	14	14	14	13	13
1 µs	13	13	14	13	14	14	14	14	14	14	14
10 µs	14	13	15	14	14	14	14	14	14	14	14
100 µs	14	14	14	13	14	14	13	13	14	13	14
1 ms	14	14	13	15	14	14	14	14	14	14	14
Rise Time from the delay CAP output (Terminal 3)											
DTU 9											
Delay Time	Measured rise time (ns)										Average Rise Time (ns)
	1	2	3	4	5	6	7	8	9	10	
0 µs	20	20	20	20	20	20	20	20	20	20	20
1 µs	20	20	20	20	20	20	20	20	20	20	20
10 µs	20	20	20	20	21	20	20	20	20	20	20
100 µs	20	20	20	20	20	20	20	20	20	20	20
1 ms	20	20	20	20	20	20	20	20	20	19	20
Rise Time from the delay TTL output (Terminal 4)											
DTU 9											
Delay Time	Measured rise time (ns)										Average Rise Time (ns)
	1	2	3	4	5	6	7	8	9	10	
0 µs	15	16	16	16	15	16	17	17	17	17	16
1 µs	18	21	18	18	20	18	18	18	19	18	18
10 µs	19	18	20	19	19	20	20	18	19	19	19
100 µs	19	19	18	18	19	18	19	19	19	20	19
1 ms	19	20	19	19	18	18	19	19	19	18	19

C.3 DTU 10 Output Voltage Rise-times

Rise Time from the immediate CAP output (Terminal 1)											
DTU 10											
Delay Time	Measured rise time (ns)										Average Rise Time (ns)
	1	2	3	4	5	6	7	8	9	10	
0 µs	16	16	16	16	16	15	16	15	15	16	16
1 µs	16	16	16	16	16	16	17	15	16	16	16
10 µs	16	16	16	16	16	16	16	16	16	16	16
100 µs	15	16	16	16	16	15	16	15	16	16	16
1 ms	17	16	16	17	16	16	16	16	17	16	16
Rise Time from the immediate TTL output (Terminal 2)											
DTU 10											
Delay Time	Measured rise time (ns)										Average Rise Time (ns)
	1	2	3	4	5	6	7	8	9	10	
0 µs	16	16	14	15	15	16	16	15	14	14	15
1 µs	13	14	14	13	14	14	14	14	14	14	14
10 µs	14	14	14	14	15	15	14	14	14	14	14
100 µs	14	15	15	15	14	14	14	15	15	14	15
1 ms	14	15	15	14	15	14	15	14	15	14	15
Rise Time from the delay CAP output (Terminal 3)											
DTU 10											
Delay Time	Measured rise time (ns)										Average Rise Time (ns)
	1	2	3	4	5	6	7	8	9	10	
0 µs	20	19	20	19	19	19	19	19	19	19	19
1 µs	20	20	19	20	20	20	20	19	20	20	20
10 µs	20	19	20	19	20	20	20	20	20	20	20
100 µs	20	19	20	20	20	20	20	20	20	20	20
1 ms	20	20	20	20	20	20	20	20	20	20	20
Rise Time from the delay TTL output (Terminal 4)											
DTU 10											
Delay Time	Measured rise time (ns)										Average Rise Time (ns)
	1	2	3	4	5	6	7	8	9	10	
0 µs	16	16	16	16	16	16	16	15	17	16	16
1 µs	16	18	17	17	18	19	17	17	18	18	17
10 µs	18	18	16	17	16	16	18	17	16	18	17
100 µs	17	17	17	18	17	17	15	17	16	16	17
1 ms	17	16	16	16	16	18	17	18	18	16	17

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19. ABSTRACT

This paper reports on tests conducted to validate the accuracy of Defence Science and Technology Group, Maritime Division's Delay Trigger Units (DTUs). The DTUs are designed to generate voltage signals to activate (trigger) external devices, such as firing units, high speed video, and data acquisition equipment in a predetermined and precise time sequence to permit the capture of data from transient events. To ensure the validity of the data obtained, the accuracy of the DTUs was evaluated against design specifications. The tests show that the DTUs met the specified requirements for the delay and rise times of the trigger signals from both the transistor to transistor logic (TTL) output signal and the 100 volt capacitor discharge output signal.